ST13P10D

P Channel Enhancement Mode MOSFET

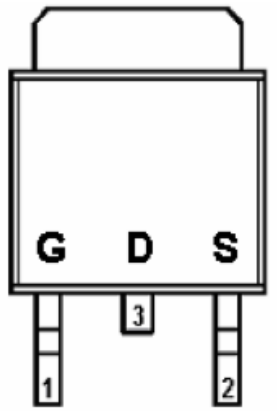
-13.0A

DESCRIPTION

ST13P10D is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The ST13P10D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or onventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

TO-252

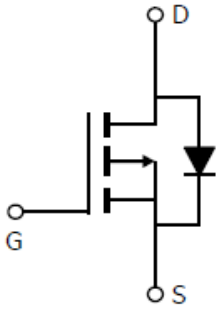


FEATURE

- -100V/-13.0A, $R_{DS(ON)}$ = 130mΩ @V_{GS} = -10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design

PART MARKING

Y: Year Code
A: Process Code
B : Wafer Code



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-100	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=100℃	ID	-13.0 -8.2	A
Pulsed Drain Current		IDM	-52	A
Continuous Source Current (Diode Conduction)		IS	-13	A
Power Dissipation	TA=25℃	PD	66	W
Operation Junction Temperature		TJ	150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	110	℃/W

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V			-25	uA
		V_{DS}=-80V,V_{GS}=0V T_J=150℃			-250	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-13A		115	130	mΩ
Forward Transconductance	gfs	V_{DS}=-50V,I_D=-7.8A	3.2			S
Diode Forward Voltage	V_{SD}	I_S=-7.8A,V_{GS}=0V			-1.6	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-80V,V_{GS}=-10V I_D=-8.4A			58	nC
Gate-Source Charge	Q_{gs}				8.3	
Gate-Drain Charge	Q_{gd}				32	
Input Capacitance	C_{iss}	V_{DS} =-25V,V_{GS}=0V F=1MHz		760		pF
Output Capacitance	C_{oss}			260		
Reverse TransferCapacitance	C_{rss}			170		
Turn-On Time	$t_{d(on)}$	V_{GS}=-10V,V_{DD}=-50V R_D=6.2Ω,R_G=9.1Ω		15		nS
	tr			58		
Turn-Off Time	$t_{d(off)}$			45		
	tf			46		

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TYPICAL CHARACTERICTICS

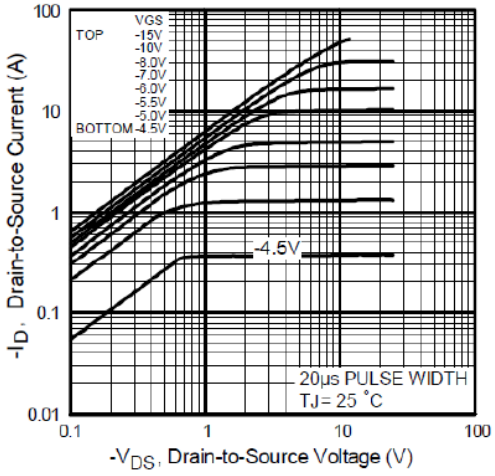

Fig 1. Typical Output Characteristics

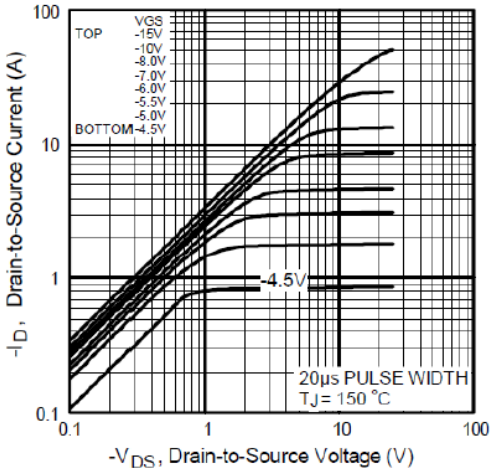

Fig 2. Typical Output Characteristics

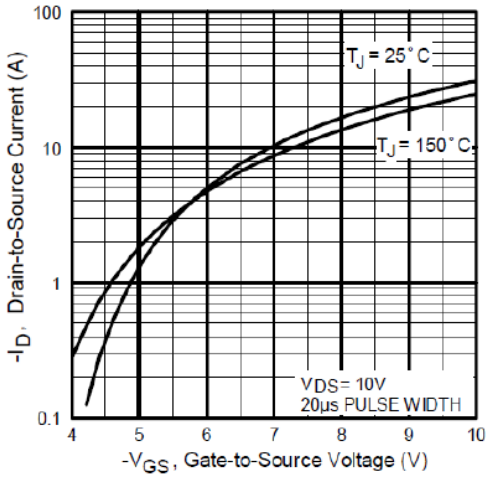

Fig 3. Typical Transfer Characteristics

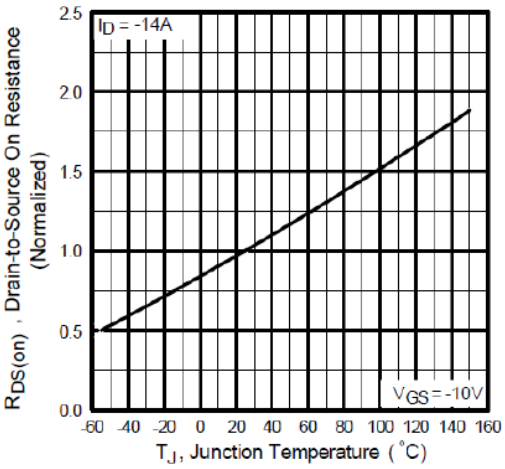

Fig 4. Normalized On-Resistance Vs. Temperature

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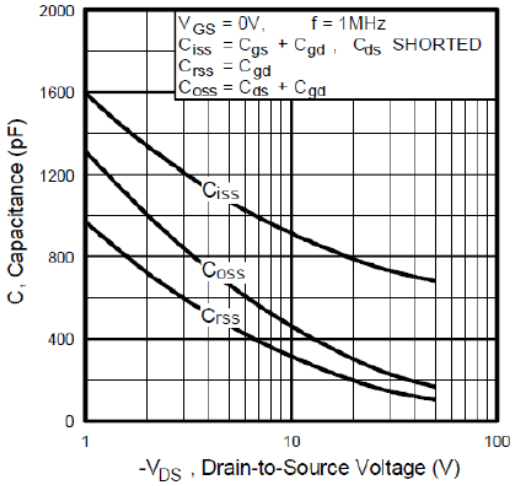


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

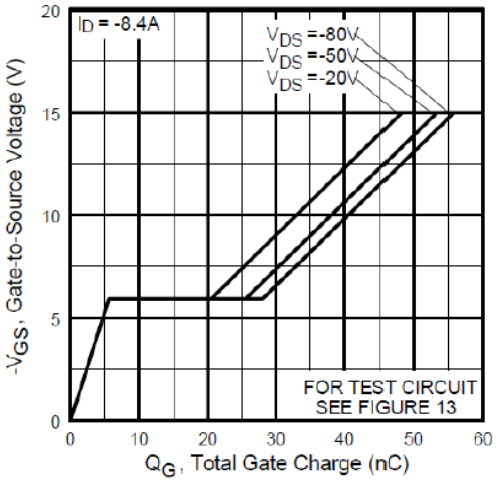
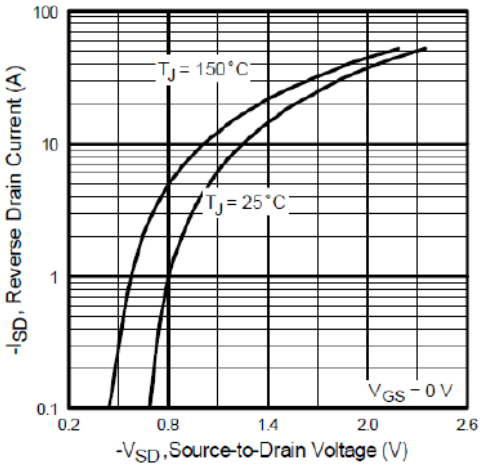
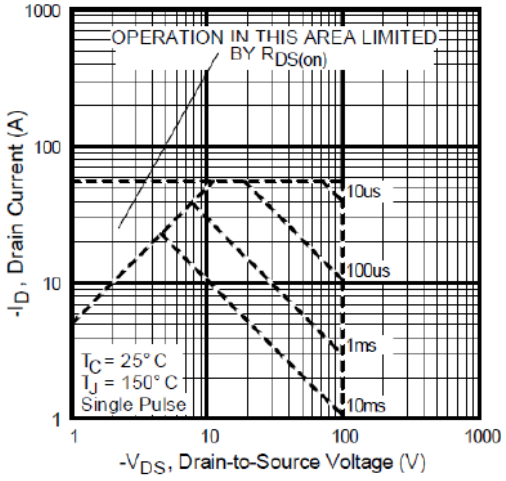


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage





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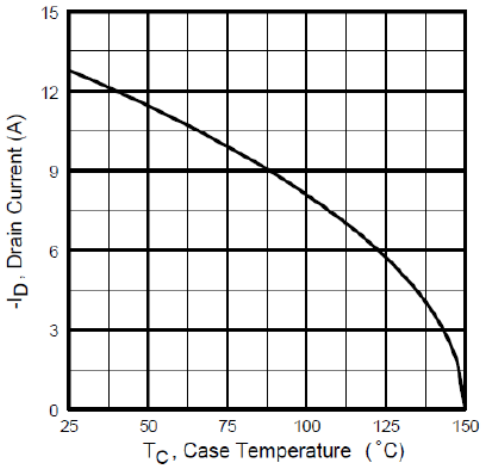

Fig 9. Maximum Drain Current Vs. Case Temperature

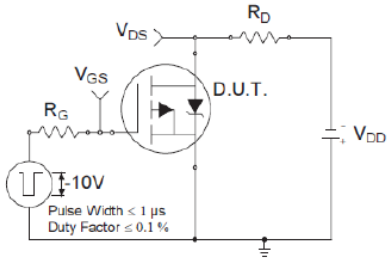

Fig 10a. Switching Time Test Circuit

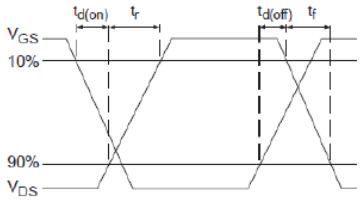

Fig 10b. Switching Time Waveforms

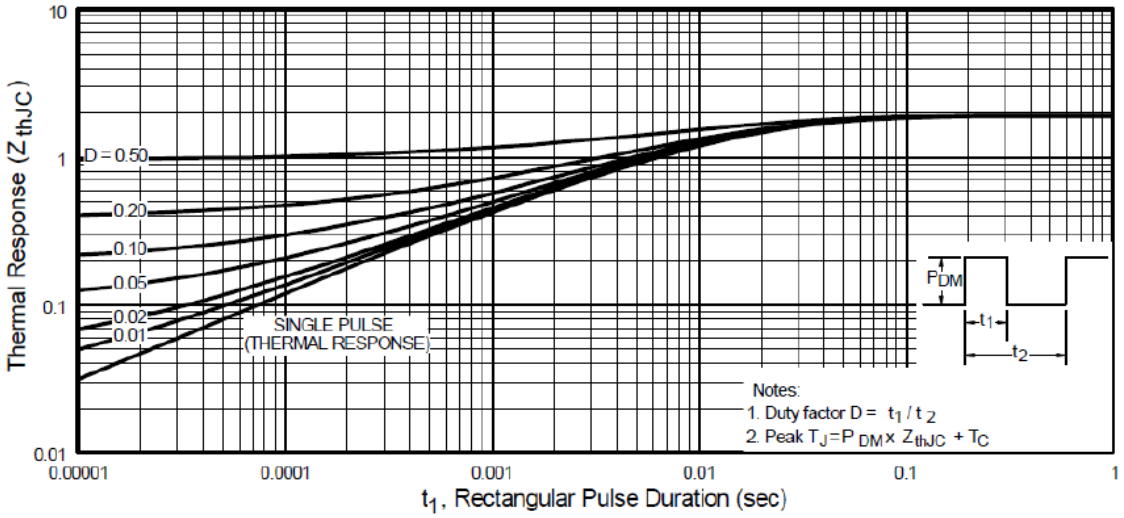

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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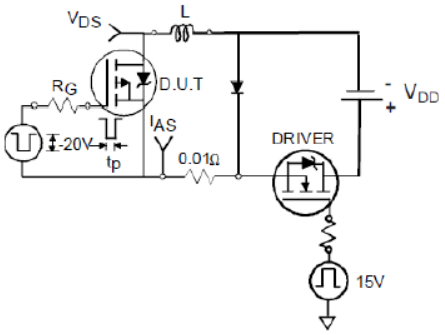

Fig 12a. Unclamped Inductive Test Circuit

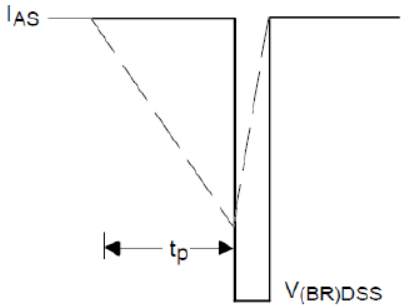

Fig 12b. Unclamped Inductive Waveforms

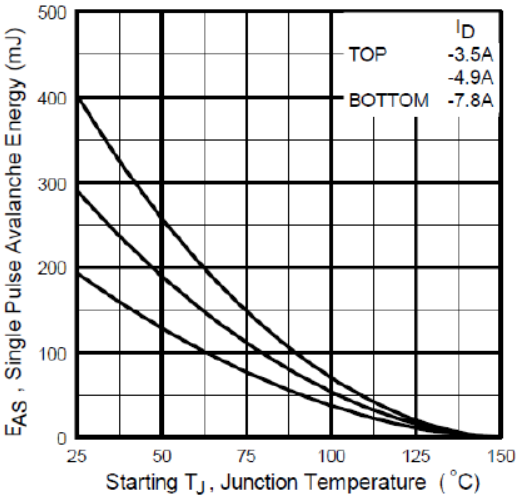

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

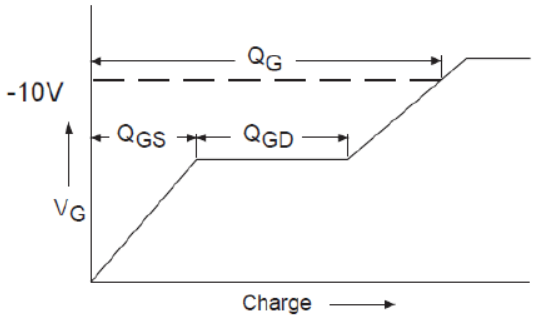

Fig 13a. Basic Gate Charge Waveform

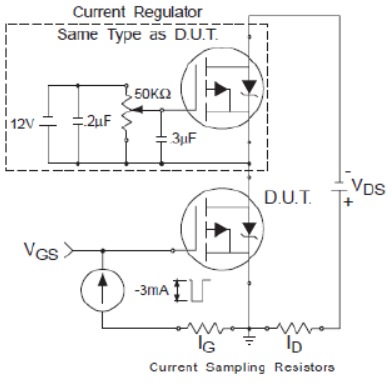

Fig 13b. Gate Charge Test Circuit

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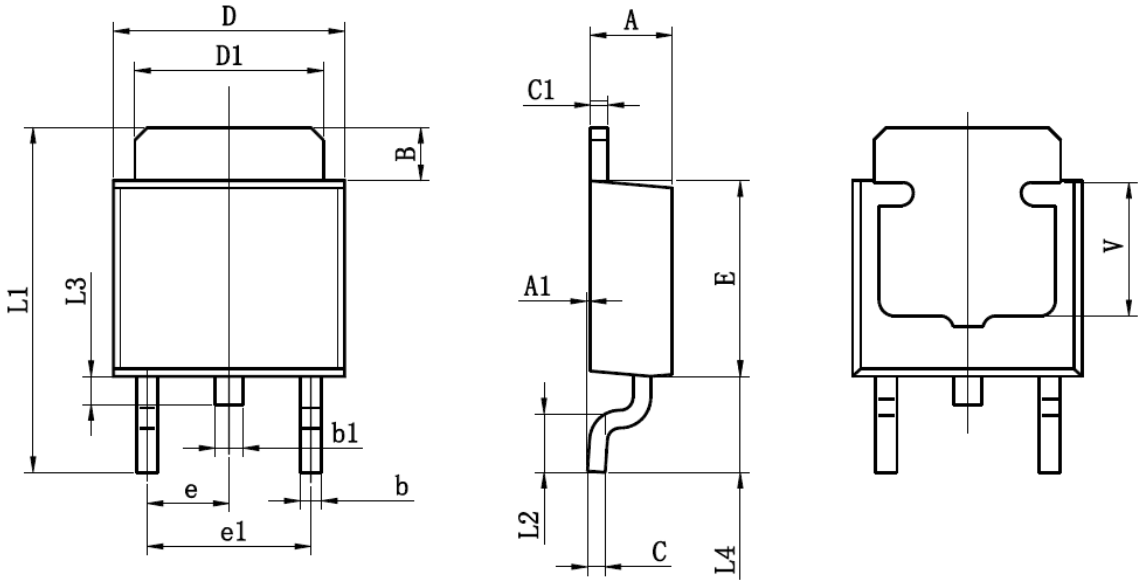
TO-252-2L PACKAGE OUTLINE SOP-8P



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

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